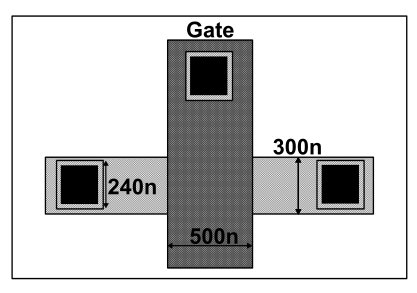
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| 浙江大学信息与电子工程学院 | **集成电路原理与设计** | 2023年10月 |
| 2023-2024学年春夏学期 |

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**Exercise 1**

1. Two layouts of n-channel MOSFET are shown in Fig.1.1. What is the width and length of the two devices?

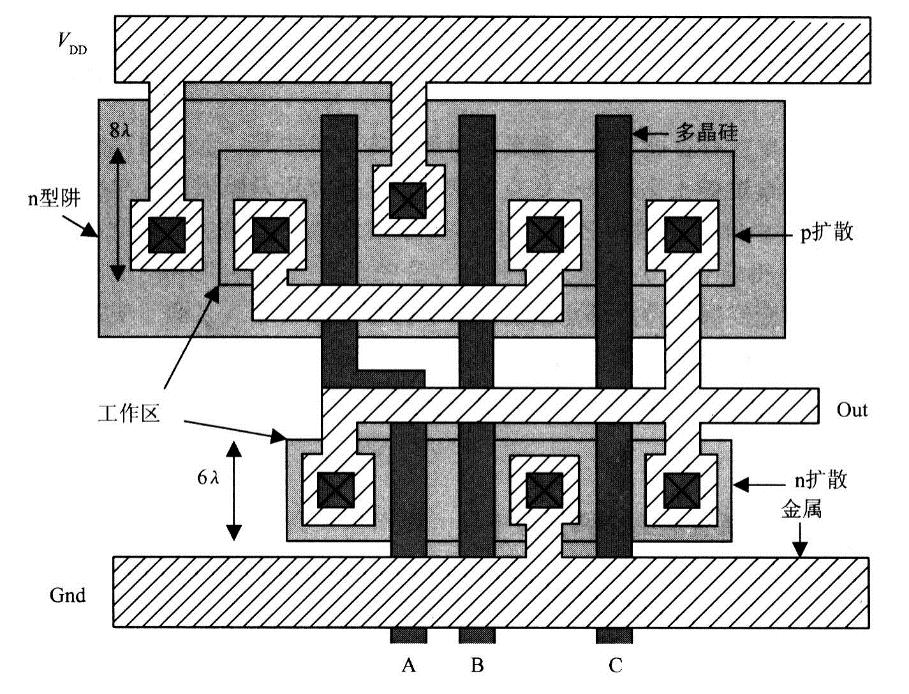
 

1. (b)

Fig.1.1

***Answer:***

1. Length=500n; Width=300n
2. Length=; Width=
3. The layouts of a circuit are shown in Fig.1.2. Give the corresponding schematics and its function, and mark the *W*/*L* sizes of each transistor. Assume *L*=2*λ*，*λ*=0.4μm.



1. **p-sub, n-well technology**



**(b) dual-well technology, and**

Fig.1.2

***Answer:***

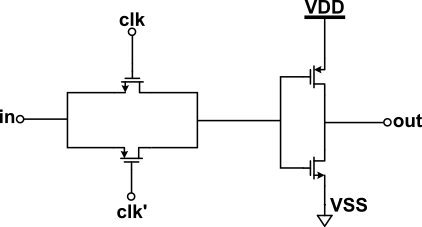
(a)



Out=

W/L of N-MOSFET: 

W/L of P-MOSFET: 



CLK high: Out=

CLK low: Out=0

W/L of N-MOSFET:

W/L of P-MOSFET:

1. Layout of a different pair with PMOS current source loads in p-sub N-well technology is shown as Fig.1.3. Give the corresponding schematics and mark the W/L sizes of each transistor. Assume λ=0.4μm.

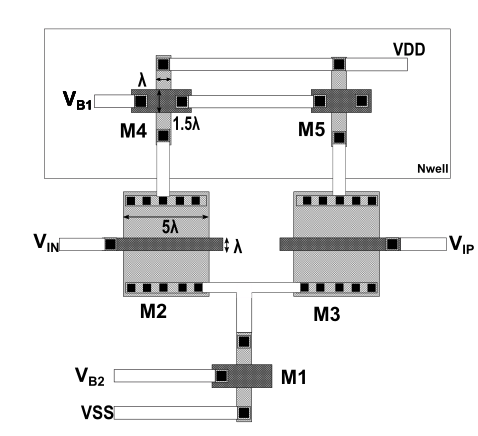
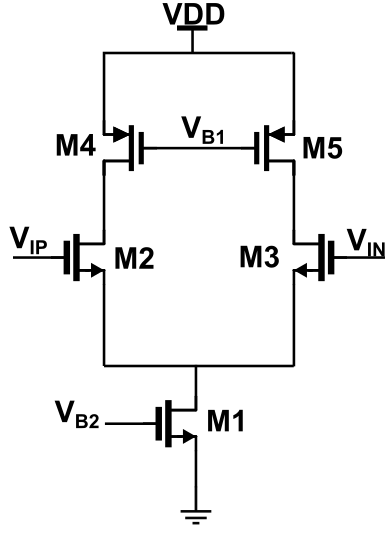


Fig.1.3

***Answer:***



**M1=M4=M5**

**M2=M3**